PRODUCT BRIEF - WIRELESS

5G mmWave System Test Platform

Simplify your 5G NR mmWave system integration

Getting a complete 5G solution to the market is both time-consuming and costly.
To test your 5G mmWave RFIC you need expensive solutions with a lot of adjacent equipment. We now give you the possibility to leverage on our integration test platform to drastically save costs and simplify the system integration.

Sivers Semiconductors has developed a 5G mmWave System Platform including our 5G New Radio (NR) Beamforming RFIC, our patch antenna RF module and the Xilinx Radio Frequency System-on-Chip (RFSoC). The platform includes a modem simulation framework in Matlab which allows radio performance evaluation using real 5G NR waveforms. Leverage on our integration test platform to drastically simplify the System integration of your 5G NR mmWave System.

Key features

- Operating frequency range: 24-29.5 GHz and prepared for 57-71 GHz (pre-3GPP R17 support)
- Radio calibration
- 5G NR frame structure and waveform
- Electronic beam forming
- Modulation up to 256 QAM
- Subcarrier spacing up to 120 kHz
- Channel bandwidth up to 400 MHz
- Figures of Merit:
  - EVM
  - Spectrum
  - Packet Error Rate
- RX AGC
- Compensation algorithms for analogue impairments:
  - RX DC offset compensation
  - IQ compensation TX and RX
  - Phase noise compensation and channel estimation
  - Frequency offset and Channel estimation
- RFIC control:
  - Matlab Via SPI
  - FPGA through GPIO

Transmitter Side

5G NR waveforms with different configurations may be generated in the modem simulation framework and uploaded to the RFSoC. The waveform/IQ samples are then transmitted through the data-converters to the Radio Frequency Integrated Circuit (RFIC). The RF Module EVKs are "plug and play" platforms, including patch antennas to evaluate the Sivers Semiconductors beam steering RFICs - TRX BF/01 for unlicensed 5G (IEEE 802.11ad) and TRX BF/02 for licensed 5G.

Receiver Side

The data received by the RFIC is sampled into the RFSoC. Some basic RFIC control is performed real-time in the FPGA logic (Gain control and beamforming), before the data is passed on to the modem simulation framework for decoding and calculation of figures of merit.